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Semiconductor Assemblies, Methods of Forming Structures Over Semiconductor Substrates, and Methods of Forming Transistors Associated with Semiconductor Substrates

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Semiconductor Assemblies, Methods of Forming Structures Over Semiconductor Substrates, and Methods of Forming Transistors Associated with Semiconductor Substrates

TECHNICAL FIELD

The invention pertains to methods of forming structures over semiconductor substrates, and in particular embodiments pertains to methods of forming transistors associated with semiconductor substrates. The invention also pertains to semiconductor assemblies.

BACKGROUND OF THE INVENTION

There are numerous applications in semiconductor processing in which it is desired to form conductive layers over oxides. For instance, transistor structures frequently comprise conductive layers formed over silicon dioxide (commonly referred to as a gate oxide). In some instances, the conductive materials comprise conductively doped silicon, and in such instances dopant can occasionally migrate through the oxide into an underlying substrate. In particular transistor devices, such dopant migration can be problematic. For instance, PMOS devices comprise an n-type channel region underneath a gate oxide, and can comprise p-type doped silicon over the gate oxide. If p-type dopant migrates from the silicon, through the oxide, and into the underlying substrate it will change the doping within the n-type channel. Such change can affect,

and even destroy, electrical properties of the transistor. Accordingly, it can be desired to alleviate dopant migration relative to PMOS devices.

In contrast to the above-discussed problems which can be associated with PMOS devices, dopant migration is typically not problematic relative to NMOS devices. However, NMOS devices can have their own associated problems. For instance, it can be desired to form gate oxide for NMOS devices which is thicker than that utilized for PMOS devices. Such can be problematic in semiconductor wafer processing, in that both NMOS devices and PMOS devices are frequently formed over the same wafer. It would be desired to develop methodology which enables different gate oxide thicknesses to be associated with different transistors on the same wafer, and in particular applications desired to develop methodology to enable NMOS transistors to have thicker gate oxide than PMOS transistors.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming a structure over a semiconductor substrate. A silicon dioxide containing layer is formed across at least some of the substrate. Nitrogen is formed within the silicon dioxide containing layer. Substantially all of the nitrogen within the silicon dioxide is at least 10Å above the substrate. After the nitrogen is formed within the silicon dioxide layer, conductively doped silicon is formed on the silicon dioxide layer.

In another aspect, the invention encompasses a method of forming a pair of transistors associated with a semiconductor substrate. First and second regions of the substrate are defined. A first oxide region is formed to cover at least some of the first region of the substrate, and to not cover the second region of the substrate. Nitrogen is formed within the first oxide region. After the nitrogen is formed, a first conductive layer is formed over the first oxide region. The first conductive layer does not cover the second region of the substrate. After the first conductive layer is formed, a second oxide region is formed over the second region of the substrate. A second conductive layer is formed over the second oxide region. The first conductive layer is patterned into a first transistor gate, and the second conductive layer is patterned into a second transistor gate. First source/drain regions are formed proximate the first transistor gate, and the second source/drain regions are formed proximate the second transistor gate.

In other aspects, the invention pertains to semiconductor assemblies.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, cross-sectional view of semiconductor wafer fragments at a preliminary processing step of a method of the present invention.

Fig. 2 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 6.

Fig. 8 is a diagrammatic, cross-sectional view of an apparatus which can be utilized in methodology of the present invention.

Fig. 9 is a diagrammatic, cross-sectional view of another apparatus which can be utilized in methodology of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Fig. 1 shows a semiconductor wafer 10 at a preliminary processing step of the present invention. Wafer 10 comprises a substrate 16 which is divided into a first region 12 and a second region 14. Substrate 16 can comprise, for example, monocrystalline silicon lightly doped with a background p-type dopant. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Regions 12 and 14 can correspond to differently-doped regions of substrate 16. For instance, region 12 can correspond to a portion of substrate 16 having a heavier concentration of n-type conductivity enhancing dopant than p-type conductivity enhancing dopant, and can accordingly be referred to as an n-type doped region. Further, region 14 can correspond to a region of substrate 16 wherein the p-type

dopant concentration is heavier than any n-type dopant concentration, and can accordingly be referred to as a p-type region of substrate 10. In order to emphasize this aspect of the invention and assist in the description that follows, substrate 16 of region 12 is labeled with an "n", and region 14 is labeled with a "p". It is to be understood that the shown doping of regions 12 and 14 corresponds to a particular embodiment of the present invention, and that other embodiments are encompassed wherein both of regions 12 and 14 are similarly doped, including embodiments wherein regions 12 and 14 are both heavier doped with n-type dopant than p-type dopant, as well as embodiments wherein regions 12 and 14 are both heavier doped with p-type dopant than n-type dopant.

In particular embodiments of the present invention, regions 12 and 14 correspond to portions of a semiconductor memory assembly, and in such embodiments regions 12 and 14 can both correspond to memory array regions, or can both correspond to regions peripheral to a memory array regions, or alternatively one of regions 12 and 14 can correspond to a memory array region while the other regions 12 and 14 corresponds to a portion of the wafer peripheral to the memory array region.

An oxide layer 18 is formed over substrate 16. Oxide layer 18 can comprise, for example, silicon dioxide and can be formed by chemical vapor deposition over layer 16. Alternatively, if substrate 16 comprises silicon (such as, for example, if substrate 16 is monocrystalline

silicon) a silicon dioxide layer 18 can be formed by oxidizing an upper surface of substrate 16.

Nitrogen is shown being dispersed onto and within layer 18. The nitrogen is preferably formed primarily at a surface of oxide layer 18. Layer 18 is preferably less than 50Å thick, and in particular embodiments is about 40Å thick. Preferably, an entirety of the nitrogen formed within layer 18 is at least 10Å above substrate 16. Alternatively, substantially all of the nitrogen formed within layer 18 is preferably at least 10Å above substrate 16. For purposes of interpreting this document and the claims that follow, it is to be understood that the reference to "substantially all" of the nitrogen within silicon dioxide layer 18 being at least 10Å above substrate 16 is defined to indicate that no measurable amount of nitrogen is in the portion of layer 18 that is within 10Å of substrate 16. In particular embodiments of the present invention, substantially all of the nitrogen formed within layer 18 is formed within the top 10Å of layer 18. In other words, no measurable amount of nitrogen extends below the top 10Å of layer 18, which can, in particular embodiments, indicate that an entirety of the nitrogen is within the top 10Å of layer 18.

Figs. 8 and 9 illustrate apparatuses which can be utilized for forming nitrogen within only the upper portions of silicon dioxide layer 18. Referring to Fig. 8, nitrogen-comprising region 22 can be formed by remote plasma nitridization utilizing an apparatus 200.

Apparatus 200 comprises a plasma chamber 202 and a reaction chamber 204. Reaction chamber 204 comprises a substrate holder 206, and substrate 16 is supported within chamber 204 by holder 206. Preferably, holder 206 is configured to rotate substrate 16 during exposure of substrate 16 to activated nitrogen species. Such activated nitrogen species are formed within plasma chamber 202 by, for example, exposing N_2 and/or other nitrogen-containing materials (such as N_2O or NH_3) to plasma conditions, with the term "activated" indicating that the nitrogen species is different than the form of nitrogen fed to the plasma. An activated nitrogen species can comprise, for example, a nitrogen ion or a nitrogen atom in an energy state higher than its ground state. Exemplary plasma conditions comprise utilization of a microwave plasma generator at a power of from about 1,500 watts to about 3,000 watts, and utilizing a pressure within chamber 202 of less than or equal to about 3 Torr. The plasma of chamber 202 forms activated nitrogen species which migrate along a passageway 208 into chamber 204 whereupon the species can form a nitrogen-comprising layer over and within oxide 18 (Fig. 1).

An arrow is shown within passageway 208 to indicate migration of plasma activated nitrogen species through passageway 208. Preferably, passageway 208 is of sufficient length so that plasma 202 is at least about 12 inches from substrate 16. Such can enable highly activated nitrogen species formed within a plasma to relax prior to interaction with

substrate 16, which can limit penetration of the nitrogen species into substrate 16 relative to an amount of penetration which would occur with more highly activated species. In order to further limit penetration of nitrogen species into substrate 16, substrate 16 is preferably not biased relative to the plasma within chamber 202.

Suitable operating conditions for forming a nitrogen-comprising plasma over substrate 16 can include maintaining a temperature of substrate 16 at from about 550°C to about 1,000°C, rotating the wafer at about 90 rotations per minute (RPM), maintaining a pressure within chambers 202 and 204 of from about 0.8 Torr to about 2.8 Torr, and exposing the wafer to the nitridization conditions for from about one minute to about five minutes.

An alternative apparatus which can be utilized for forming nitrogen over and within oxide layer 18 (Fig. 1) is described with reference to Fig. 9 as apparatus 220. Apparatus 220 can be referred to as a high density plasma remote plasma nitridization (HDP-RPN) apparatus, or simply as a plasma nitridization (PN) apparatus. Apparatus 220 comprises a reaction chamber 222 having a wafer holder 224 therein. Wafer 16 is supported on holder 224. A plasma 226 is formed above substrate 16, and preferably is maintained a distance "X" from substrate 16, with distance "X" corresponding to at least about four inches. Nitrogen is introduced into plasma 226 in the form of, for example, N_2, and activated nitrogen species are formed from the

nitrogen. Suitable processing parameters for utilization of the apparatus of Fig. 9 include a wafer temperature of from 0°C to 400°C, no rotation of the substrate 16, a pressure within chamber 222 of from about 5 mTorr to about 15 mTorr (preferably of from about 5 mTorr to about 10 mTorr), and an exposure time of substrate 16 to activated nitrogen species within chamber 222 of from about 5 seconds to about 30 seconds.

Referring next to Fig. 2, a conductive layer 20 is formed over oxide 18, and a patterned masking layer 22 is formed over the portion of conductive layer 20 that is associated with region 12, while the portion of conductive layer 20 associated with region 14 remains exposed.

Conductive material 20 can comprise, for example, conductively doped silicon, such as, for example, conductively doped amorphous or polycrystalline silicon. In particular embodiments of the present invention, conductive layer 20 comprises p-type doped silicon. Conductive material 20 can also comprise metals, and/or silicides, in addition to, or alternatively to, the conductively doped silicon.

Masking layer 22 can comprise, for example, photoresist, and can be patterned by photolithographic processing.

Referring to Fig. 3, wafer fragment 10 is shown after being exposed to etching conditions which remove layers 20 and 18 from over region 14 of substrate 16. Masking layer 22 (Fig. 2) protects layers 18 and 20 from being removed over region 12 of substrate 16. In

embodiments in which oxide 18 comprises silicon dioxide and conductive material 20 comprises conductively doped silicon, a suitable etchant for removing materials 18 and 20 from over substrate 16 can comprise, for example, CF_4 and O_2.

It is noted that the structure shown in Fig. 3 can be obtained through processing methods other than that shown in Figs. 1-3. For instance, region 14 can be covered during formation of oxide layer 18 and conductive layer 20, and subsequently the cover removed from over region 14 to form a structure identical to that shown in Fig. 3.

Referring to Fig. 4, wafer 10 is shown after being exposed to oxidizing conditions. The oxidizing conditions form an oxide layer 24 over substrate 16, and also form an oxide layer 26 over conductive material 20. If substrate 16 comprises monocrystalline silicon and conductive material 20 comprises conductively doped silicon, oxide layers 24 and 26 will comprise silicon dioxide. Oxide layers 24 and 26 can be formed by methods other than oxidation of layer 20 and substrate 16, such as, for example, by chemical vapor deposition of silicon dioxide. Also, it is noted that the invention encompasses embodiments wherein oxide is not formed over layer 20, such as, for example, embodiments in which oxide layer 24 is formed by oxidation of substrate 16 and in which layer 20 comprises a non-oxidizable material.

Oxide layer 24 can be formed to be a different thickness than oxide layer 18. For instance, oxide layer 18 can be optimized for

formation of a PMOS transistor, and accordingly can be less than 50Å thick, and, for example, about 40Å thick, while oxide layer 24 can be optimized for formation of an NMOS transistor, and accordingly can be greater than 50Å thick, and, for example, can be about 70Å thick.

Referring to Fig. 5, a second conductive material 28 is formed over regions 12 and 14 of substrate 16. Conductive material 28 can comprise, for example, conductively doped silicon, and in particular embodiments comprises n-type doped silicon. Conductive material 28 can comprise other conductive materials in addition to, or alternatively to, conductively doped silicon, such as, for example, metals and/or silicides.

Referring to Fig. 6, wafer 10 is exposed to planarizing conditions which planarize an upper surface of wafer 10 and remove layers 26 and 28 from over first conductive layer 20. Exemplary planarizing conditions comprise chemical-mechanical polishing. Alternatively or in combination with the chemical-mechanical polishing, a polysilicon dry etch can be utilized to remove polysilicon from over both of regions 12 and 14. A suitable polysilicon dry etch is an isotropic etch utilizing HBr.

Referring to Fig. 7, layers 18 and 20 are incorporated into a first transistor structure 40 and layers 24 and 28 are incorporated into a second transistor structure 42.

First transistor structure 40 comprises a silicide layer 44 and an insulative layer 46 which are formed over layers 18 and 20 and patterned

together with layers 18 and 20 to form a gate structure. Silicide layer 44 can comprise, for example, titanium silicide or tungsten silicide.

Second transistor structure 42 comprises a silicide layer 48 and insulative layer 50 which are formed over layers 24 and 28 and patterned with layers 24 and 28 to form a gate structure. Silicide layer 48 can comprise, for example, titanium silicide or tungsten silicide, and insulative layer 50 can comprise, for example, silicon nitride.

Sidewall spacers 52 are shown formed along sidewalls of patterned materials 24, 28, 48 and 50, as well as along sidewalls of patterned materials 18, 20, 44 and 46. Spacers 52 comprise insulative materials, and can comprise, for example, silicon dioxide or silicon nitride.

It is noted that although conductive layers 44 and 48 are shown separately from conductive materials 20 and 28, silicides 44 and 48 could also have been incorporated into conductive materials 20 and 28, respectively. In other words, conductive material 20 could, in particular embodiments, encompass two layers, with a lower layer comprising conductively doped silicon and an upper layer comprising a silicide; and similarly conductive material 28 could, in particular embodiments, encompass two layers with a lower layer comprising conductively doped silicon and an upper layer comprising a silicide.

Lightly doped diffusion (Ldd) regions 54 are shown within region 12 of substrate 16, and source/drain regions 56 are also shown within region 12 of substrate 16. Source/drain regions 56 comprise p-type

dopant and together with Ldd regions 54 and layers 18, 20, 44 and 46 define a PMOS transistor 40. Lightly doped diffusion regions 54 typically comprise p-type dopant.

Lightly doped diffusion regions 58 are shown within region 14 of substrate 16 and heavily doped source/drain regions 60 are also shown within region 14 of substrate 16. Heavily doped source/drain regions 60 comprise n-type dopant, and together with layers 24, 28, 48 and 50 define NMOS transistor 42. Lightly doped diffusion regions 58 typically comprise n-type dopant.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.